REMARKS

Claims 1-41 were pending. Claims 1-8, 20, 22-24, 29-33, and 36-39 were rejected. Claims 9-19, 21, 25-28, 34, and 35 were objected to as being dependent upon a rejected base claim. Claims 40 and 41 were allowed. By the above amendment, the Applicant has amended claims 1, 4, 36, and 39. The Applicant hereby requests further consideration and re-examination in view of the amendment made above and remarks set forth below.

Specification Objections:

The specification was objected to due to informalities. The paragraph starting at page 4, line 4, was missing the U.S. Application No. The U.S. Application No. has been added by the above amendment to the specification.

Claim Objections:

The claims were objected to due to informalities. Claim 4 included the redundant term, "a logic element." The redundant term has been deleted by the above amendment to claim 4.

Additional Claim Amendments:

Claims 1, 36, and 39 have been amended to replace the word "some" with the words "at least two" to clarify that the phrase "some of the switches" means "at least two of the switches."

Claim Rejections under 35 U.S.C. § 102:

Claims 1-8, 20, 22-24, 29-33, and 36-39 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,651,013 to Iadanza. The rejection is respectfully traversed.

Iadanza teaches a programmable gate array (10) that includes logic cells (20), an interconnect network, (22a) and (22b), and a scan chain (34). (Col. 5, lines 43-59.) Iadanza teaches that each logic cell (20) includes input multiplexing (64), combinational logic (68), a storage circuit (50), and output multiplexing (66). (Col. 6, lines 33-48, and Fig. 4.) The input multiplexing (64) and output multiplexing (66) of each logic cell (20) connect the logic cell (20) to the interconnect network (22). (Col. 6, lines 33-36, and Fig. 4.) The combinational logic (68) of each logic cell (20)

performs logic functions on a logic input signal to produce a resultant logic signal (62). The resultant logic signal (62) is stored in the storage circuit (50) before it is transmitted to the interconnect network (22) as an output (60) by way of the output multiplexing (66). (Col. 6, lines 38-44, and Fig. 4.)

Iadanza refers the reader to several incorporated by reference U.S. Patent Application Nos. for details regarding the interconnect network, (22a) and (22b). (Col. 5, lines 49-53.) Based on the titles provided by Iadanza, it appears that U.S. Patent Application No. 08/459,579, filed on Jun. 2, 1995, which issued as U.S. Patent No. 5,631,578 to Clinton *et al.* on May 20, 1997, is the appropriate reference for determining details regarding the interconnect network, (22a) and (22b). (Iadanza, col. 1, lines 5-23.) U.S. Patent No. 5,631,578 to Clinton *et al.* is provided on an Information Disclosure Statement with this response.

Iadanza teaches that the scan chain (34) may include several integrated circuits, (32a-f), one or more of which are a programmable array, or that the scan chain is an individual scan chain for a programmable array. (Col. 5, line 54, to col. 6, line 2.) The scan chain (34) is used for boundary scan or level sensitive scan testing. (Col. 5, lines 57-59, and col. 6, lines7-22.) The storage circuit (50) of logic cell (20) performs as a shift register stage within the scan chain in which the storage circuit (50) has a scan input (52), a scan output, and inputs for A, B, and C clock signals. (Col. 6, lines 42-47, and Fig. 4.) The storage circuits (50) of logic cells (20) of a programmable array (10) can be connected together to form the scan chain using each storage circuit's scan input and scan output. (Col. 6, lines 52-55.)

Iadanza further teaches that the storage circuit (50), which is also referred to as a shift register stage of the scan chain, includes a master section (120), a slave section (122), and a programmable switch (100). (Col. 6, lines 59-61, and col. 7, lines 12-14, and Figs. 4 and 5.) If the C type clock signal is provided to the master section (120), the resultant logic signal (62) proceeds through the master and slave sections, (120) and (122), on its way to the output multiplexing (66) of a logic cell (20). If the A type clock signal is provided to the master section (120), the scan input proceeds through the master and slave sections, (120) and (122), of a logic cell (20) to become a scan output. The scan output then becomes a scan input for the next storage circuit (50) in the scan chain. The selection of the C type clock signal or the A type clock signal determines whether the resultant logic signal or the scan input, respectively, enters the storage circuit (50) and proceeds to the slave section (122). The B type clock signal

merely determines the timing of transferring the contents of the slave section onward. (Col. 6, line 66, to col. 7, line 11, and Figs. 4 and 5.) The scan output and the conductor that couples the slave section (122) to the output multiplexing (66) are two branches of a single output. (Figs. 4 and 5, ref. nos. 58 and 60.)

The programmable switch (100) of the storage circuit (50) allows a selection of an alternative clock signal from an alternative clock source (56) to use in lieu of the B or C type clock signals. (Col. 7, lines 14-18, and Fig. 5.)

According to claim 1, the present invention is a reconfigurable device that comprises tiles and an interconnect architecture. Each of the tiles comprises a circuit. The interconnect architecture couples to the circuit of each tile and comprises switches and registers. In operation at least two of the switches route a signal from a first tile to a second tile along the interconnect architecture and at least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period.

Claim 1 is rejected under 35 U.S.C 102(b) as being anticipated by Iadanza, which is respectfully traversed. The rejection identifies the logic cell (20) as a tile comprising a circuit (68) and further identifies the master and slave sections, (120) and (122), and the switch (100) as an interconnect architecture, which is incorrect.

The master and slave sections, (120) and (122), and the switch (100) are components of the storage circuit (50). For several reasons, the storage circuit (50) is an integral part of the circuit of the logic cell (20) and, thus, cannot be part of the claimed "interconnect architecture." First, Iadanza teaches that each logic cell sequentially includes the input multiplexing, the combinational logic, the storage circuit, and the output multiplexing. The input multiplexing receives the input logic signal, the combinational logic transforms the input logic signal to the resultant logic signal, the storage circuit stores the resultant logic signal, and finally the output multiplexer transmits the resultant logic signal to the interconnect network. Since the storage circuit couples the input multiplexing to the output multiplexing of a logic cell, the storage circuit is an integral part of the circuit of the logic cell.

Second, Iadanza teaches that a logic cell is coupled into the scan chain by the storage circuit. Since the storage circuit is the only component of the logic cell that is coupled into the scan chain, the storage circuit is an integral part of the logic cell.

Third, as described above, there are two types of signals that move through a logic cell (20). The first type of signal is a logic signal that enters the logic cell at the

input multiplexing (64). The combinational logic (68) then transforms the logic signal into a resultant logic signal and passes the resultant logic signal to the storage circuit. The storage circuit (50) then provides the resultant logic signal to the output multiplexing (66), which transfers it to the interconnect network (22). The second type of signal is a scan signal that enters the logic cell via the scan input of the storage circuit (50) and exits the logic cell via the scan output the storage circuit (50). Again, this means that the storage circuit (50) is an integral part of the logic cell. Thus, applying claim 1 to the programmable array (10), "tiles each comprising a circuit" are the logic cells each comprising the master and slave sections, (120) and (122), and the switch (100) (i.e., the storage circuit (50)).

The tiles of claim 1 are separate elements from the interconnect architecture of claim 1. While there are undoubtedly circumstances where it is unclear where one element ends and another element begins, this is not the situation here. Since the master and slave sections, (120) and (122), and the switch (100) form part of Iadanza's logic cells, they cannot also be part of the interconnect architecture. Therefore, Iadanza does not teach this feature of claim 1. Iadanza does briefly teach an interconnect network and refers to Clinton *et al.* for details of the interconnect network. A review of the teachings by Clinton *et al.* failed to uncover the limitations of the interconnect architecture of claim 1.

Further, the rejection identifies the programmable switch (100) as switches that route a signal from a first tile to a second tile, which is incorrect. To route a signal from the first tile to the second tile is to select the signal's path when traveling from the first tile to the second tile. As described above, the programmable switch (100) taught by Iadanza allows switching to an alternate clock source in lieu of the C type clock or the B type clock. The programmable switch (100) taught by Iadanza does not perform any type of switching function on the logic signal (62) or the scan signal (52). Thus, the programmable switch (100) does not route a signal.

For several reasons, the storage circuit (50) is not "at least two switches that route a signal from a first tile to a second tile along the interconnect architecture." First, assuming that the storage circuit can be categorized as a switch that selects a logic signal or a scan signal means that it can be only one switch. If the C type clock signal is applied to the master section, it selects the logic signal, and if the A type clock signal is applied to the master section, it selects the scan signal. Because the storage circuit selects one of two signals, it is at most a single switch.

Second, the storage circuit *selects* one of two signals; it does not *route* a signal from a first tile to a second tile. The verb "to route" means to select a direction. Regardless, of whether the logic signal (62) or the scan signal (52) is selected by the storage circuit, the signal exiting the slave section proceeds to both the output multiplexing and the scan output since the scan output and the conductor coupling the slave section to the output multiplexing are two branches of a single output. No direction is selected.

Third, claim 1 requires that "at least two switches ... route a signal along the interconnect architecture," which means that a first switch must select a first direction and a second switch must select a second direction as the signal proceeds through the interconnect architecture. There are no first and second switches, only a single switch. There is no routing of a signal, only a selection from two signals. Since there is no routing, there is no selection of a first direction and no selection of a second direction. And, as described above, the storage circuit (i.e., a selection switch as opposed to a routing switch) is not located along the interconnect architecture; it is an integral part of the tile).

Thus, for at least these reasons, claim 1 is allowable over Iadanza. Claims 2-8, 20, 22-24, and 29-33 are allowable at least because they depend from an allowable base claim 1.

According to claim 36, the present invention is a reconfigurable device that comprises tiles and an interconnect architecture. Each of the tiles comprises a circuit and a tile size. The tile size allows a first signal to traverse the circuit within about a repeating time period. The interconnect architecture couples to the circuit of each tile and comprises switches and registers. In operation at least two of the switches route a second signal from a first tile to a second tile along the interconnect architecture and at least two of the registers consecutively latch the second signal at a time interval of no more than the repeating time period.

As described above relative to claim 1, Iadanza and Clinton *et al.* fail to teach the limitations of the interconnect architecture. Since the storage circuit (50) taught by Iadanza forms part of the logic cell (20), which is the equivalent to the tiles of claim 36, it cannot also be part of the interconnect architecture of claim 36. Further, the programmable switch (100) switches between an alternative clock signal and the B or C type clock signal. And, as described above, Iadanza fails to teach "at least two

switches that route a signal from a first tile to a second tile along the interconnect architecture." For at least these reasons, claim 36 is allowable over Iadanza.

Claims 37 and 38 are allowable at least because they depend from an allowable base claim 36.

According to claim 39, the present invention is a reconfigurable device that comprises tiles and an interconnect architecture. Each of the tiles comprises a circuit. The interconnect architecture couples to the circuit of each tile and comprises switches and registers. In operation at least two of the switches route a signal from a first tile to a second tile along the interconnect architecture and at least two of the registers consecutively latch the signal at a time interval of no more than a clock cycle period.

As described above relative to claim 1, Iadanza and Clinton *et al.* fail to teach the limitations of the interconnect architecture. Since the storage circuit (50) taught by Iadanza forms part of the logic cell (20), which is the equivalent to the tiles of claim 39, it cannot also be part of the interconnect architecture of claim 39. Further, the programmable switch (100) switches between an alternative clock signal and the B or C type clock signal. And, as described above, Iadanza fails to teach "at least two switches that route a signal from a first tile to a second tile along the interconnect architecture." For at least these reasons, claim 39 is allowable over Iadanza.

Conclusion:

In view of the above, the Applicant submits that all of the pending claims are now allowable. Allowance at an early date would be greatly appreciated. Should any outstanding issues remain, the Examiner is encouraged to contact the undersigned at (408) 293-9000 so that any such issues can be expeditiously resolved.

Respectfully Submitted,

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Derek J. Westberg (Reg. No. 40,872)